UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,541	06/23/2003	Takeshi Sakata		5764

24956 7590 09/13/2006

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,541	SAKATA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/349761.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment (Preliminary Matters)

1. Claim interpretation:

The Authoritative Dictionary of IEEE Standards Terms defines "address" as inputs whose states select a particular cell or group of cells.

In addition, the last paragraph on page 2 teach that a method for storing addresses is the programmable set of fuses in Figure 2 of the Applicant's own specification for connecting input addresses DA0 to DA1 to repair-decision results RH0 to RH3 (Note Figures 3-6 of the Applicant's disclosure teach alternate programming means for generating repair-decision results RH0 to RH1 based on a defective address). The Examiner asserts that Figures 2-6 of the Applicant's specification teach "storing a defect address" as one of ordinary skill in the art at the time the invention was made would use the language to describe the effect of rerouting a logical address to avoid using defective memory by storing physical address information pertaining to the defective memory since the programmable fuses and logic of Figures 2-6 store Binary information based on a physical address locations of defective memory and are used to avoid writing to defective memory by rerouting physical address lines to replacement memory. Since the stored binary information provides inputs to other circuitry which effectively select replacement memory cells, the binary information stored in the programmable fuse is an address by definition and since it is binary address information that avoids the use of defective memory it is a defect address by English construction since defect is

used as an adjective to indicate a relationship. Hence by Definition, English construction and the Applicant's own use of the term "defect address", binary information stored in a fuse array to avoid the use of defective memory is a defect address.

Prior Art teachings:

Murakami teaches a memory block addressed by a binary address of NA bits (Memory Cell Array 1 in Figure 2 is a memory block addressed by a binary address $[x_1, x_2,\ldots,x_n]$ of NA=n bits); and a defect address storing circuit including ND (ND = 2^NA) storage elements for storing NS (NS = two or more) defect addresses in relation to a plurality of defects in the memory block (Figure 3 in Murakami teaches an n=ND element switching circuit for repairing a single row error having n=ND single bit storage elements; Note: a fuse is a single bit storage element; col. 9, lines 8-46 in Murakami teaches that a single fuse fi out of the n=ND fuses is cut to store the physical defect address of the defective row being repaired in order to avoid using the defective row, redirecting logical addresses to a replacement row so that the n=ND fuses store the physical address of a defective row when a single fuse is cut; col. 15, lines 8-25 teach that the circuit of Figure 3 can be extrapolated to correct k defective rows by cascading the set of ND storage elements of Figure 3 to comprise k sets of n=ND storage elements for a total of k*n=k*ND storage elements and provides examples of how to do this in Figures 10A and 10B for k=2; Note: if $k=2^n/n=2^{ND}/ND$, then the memory can repair $k=2^n/n=2^{ND}/ND$ defective rows and has $2^n=2^{ND}$ storage elements), wherein the NS defect addresses

from said binary address of NA bits are addresses which are different from each other, and each of the ND storage elements stores one bit (Each of the spare rows in Figure 10B of Murakami is used to replace different defective rows so that each of the fuse sets comprising n=ND elements stores different defect addresses to ensure that defective rows are rerouted to replacement rows).

Response to Arguments

2. Applicant's arguments filed 08/02/2006 have been fully considered but they are not persuasive.

The Applicant contends, "Murakami is silent with respect to disclosing how many fuses are needed for storing the address and how they are programmed".

The Examiner disagrees and asserts that col. 9, lines 8-46 in Murakami teaches that a single fuse fi out of the n=ND fuses is cut to store the physical defect address of the defective row being repaired in order to avoid using the defective row, redirecting logical addresses to a replacement row. The n=ND fuses store the physical defect address of a defective row when a single fuse is cut. ND=n fuses are required to store a single defect address. Col. 15, lines 8-25 teach that the circuit of Figure 3 can be extrapolated to correct k defective rows by cascading the set of ND storage elements of Figure 3 to comprise k sets of n=ND storage elements for a total of k*n=k*ND storage elements and provides examples of how to do this in Figures 10A and 10B for k=2. To repair k defective rows, k sets of n=ND storage elements for a total of k*n=k*ND storage

elements are needed and k defect addresses are stored by cutting a single fuse in each of the k sets of ND storage elements. Murakami explicitly teaches k*n=k*ND fuses are needed for storing k defect addresses and that they are programmed to store the k defect addresses by cutting a single fuse in each of the k sets of ND storage elements.

The Applicant contends, "The fuses (fl -fn) described in Fig. 1 of Murakami do not store any address as pointed out by the Examiner, and as is clear since they are placed after the column decoder".

The Examiner disagrees and asserts that col. 9, lines 8-46 in Murakami teaches that a single fuse fi out of the n=ND fuses is cut to store the physical defect address of the defective row being repaired in order to avoid using the defective row, redirecting logical addresses to a replacement row. The Examiner asserts that a row or column decoder is used to translate logical addresses into physical addresses and the n=ND fuses in Figure 3 of Murakami are used to store a physical defect address.

The Applicant contends, "Murakami does not disclose the number of storage elements for storing a plurality of defect addresses".

Col. 15, lines 8-25 teach that the circuit of Figure 3 can be extrapolated to correct k defective rows by cascading the set of ND storage elements of Figure 3 to comprise k sets of n=ND storage elements for a total of k*n=k*ND storage elements and provides examples of how to do this in Figures 10A and 10B for k=2. To repair k defective rows, k sets of n=ND storage elements for a total of k*n=k*ND storage elements are needed

and k defect addresses are stored by cutting a single fuse in each of the k sets of ND storage elements. Murakami explicitly teaches k*n=k*ND fuses are needed for storing k defect addresses and that they are programmed to store the k defect addresses by cutting a single fuse in each of the k sets of ND storage elements.

The Applicant contends, "the reference is limited to disclosing that only one address can be repaired".

The Examiner disagrees and asserts that col. 15, lines 8-25 teach that the circuit of Figure 3 can be extrapolated to correct k defective rows by cascading the set of ND storage elements of Figure 3 to comprise k sets of n=ND storage elements for a total of k*n=k*ND storage elements and provides examples of how to do this in Figures 10A and 10B for k=2.

The Examiner disagrees with the applicant and maintains all rejections of claims 1-7. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that claims 1-7 are not patentably distinct or non-obvious over the prior art of record in view of the references, Murakami, Shuji (US 5471427 A) and Harper; Samuel D. (US 3633175 A) in view of Kato, Hideo (US 6249850 B1) and Cloud, Eugene H. et al. (US 6119251 A, hereafter referred to as Cloud) as applied in the last office action, filed 05/02/2006. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami, Shuji et al. (US 5471427 A, hereafter referred to Murakami) in view of Harper; Samuel D. (US 3633175 A).

See the Non-Final Action filed 05/02/2006 for detailed action of prior rejections.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami, Shuji (US 5471427 A) and Harper; Samuel D. (US 3633175 A) in view of Kato, Hideo (US 6249850 B1).

See the Non-Final Action filed 05/02/2006 for detailed action of prior rejections.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami, Shuji (US 5471427 A) and Harper; Samuel D. (US 3633175 A) in view of Cloud, Eugene H. et al. (US 6119251 A, hereafter referred to as Cloud).

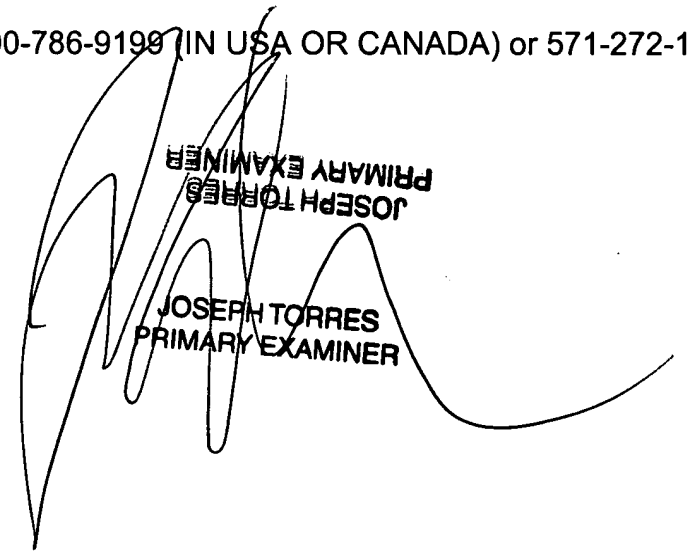
See the Non-Final Action filed 05/02/2006 for detailed action of prior rejections.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133